

Frequency performance enhancement of AlGaIn/GaN HEMTs on diamond

Q. Diduck, J. Felbinger, L.F. Eastman, D. Francis, J. Wasserbauer, F. Faili, D.I. Babić and F. Ejeckam

The performance of an AlGaIn/GaN high electron mobility transistor (HEMT) on diamond substrate is reported. Presented is a device with a gate footprint $L_G = 40$ nm and a periphery $W_G = 100$ μm that exhibits $f_T = 85$ GHz and $f_{\text{max}} = 95$ GHz. It is believed that this represents the best frequency performance of a GaN-on-diamond HEMT.

Introduction: The highly-desirable power and frequency capabilities of AlGaIn/GaN high electron mobility transistors (HEMTs) are limited by thermal performance [1]. The electron mobility of AlGaIn/GaN heterostructures is known to reduce as channel temperature increases $\tilde{\mu}T/T_0^{-1.8}$ [2]. By utilising a substrate with a high thermal conductivity, optimal performance can be extended to higher power densities. GaN-on-diamond (GaN/D) HEMTs have exhibited approximately half the thermal resistance of those on SiC substrates; thus, the GaN/D material system is expected to provide the best platform for high-performance high-power devices [3]. While extensive research has focused on GaN-on-SiC and GaN-on-sapphire materials and devices, GaN/D substrates are relatively new. This work focuses on device research in an effort to optimise the performance of HEMTs on this new material system.

The GaN/D substrate is prepared by atomically attaching GaN epitaxial layers to CVD polycrystalline diamond [4]. First, the AlGaIn/GaN epitaxial layers are grown by organometallic-vapour-phase epitaxy atop a silicon substrate. Next, this wafer is flipped and mounted onto a sacrificial carrier and the silicon substrate is etched away. Finally, the remaining AlGaIn/GaN layers are attached to polycrystalline diamond using a proprietary process. The resulting structure leaves the two-dimensional electron gas layer intact, as reported in [4].

Fabrication: The GaN/D material was prepared by Group4Labs. The epitaxial layers are composed of a 10 Å GaN cap, 175 Å $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$, and a 10 Å AlN interbarrier pseudomorphically grown on a 1.0 μm unintentionally doped GaN buffer layer and a 0.9 μm AlGaIn seed layer. A 200 Å interface layer is used to atomically bind the GaN to 75 μm polycrystalline diamond. Device formation is achieved via electron beam lithography for all lithographic steps owing to a slight bow (~ 5 μm over 15 mm) in the free-standing GaN/D wafer. The 150 nm mesa isolation was performed using an inductively-coupled plasma with $\text{Cl}/\text{BCl}_3/\text{Ar}$ chemistry. Contacts were formed using a Ta/Ti/Al/Mo/Au metal stack that was annealed until it became ohmic. The passivation layer, 60 nm of silicon nitride, was deposited using a plasma enhanced chemical vapour deposition system. Front side via access to the contacts and the passivation recess for the gates were performed using a reactive ion etch with CF_4 chemistry. The pressure, power and gas flow were adjusted to achieve 70° sloping side walls, which enabled the footprint of the gate to be scaled smaller than the pattern used to generate the recess by a factor of $\sim 2.5\times$, resulting in a 40 nm footprint. The sloping sidewalls create a V-gate structure which improves the performance of the FET by reducing fringing fields [5]. Gate metallisation was composed of 200 Å Ni, 3000 Å Cu, and 50 Å Au; copper was utilised to improve the unity current gain f_T , against a conventional Ni/Au gate stack by $\sim 20\%$ [6]. The thickness of the gold cap layer was minimised to fully utilise the copper as the main conductor, since skin effect plays a dominant role at millimetre wavelengths.

Measurements and results: Transfer length method measurements were performed using the four-point probe technique with a Keithley 236 source measurement unit. Contact resistance of 0.8 Ωmm with a sheet resistance of 800 Ω/\square was observed. All device measurements were performed on a two-finger device with total periphery $W_G = 100$ μm , a gate-drain spacing $L_{GD} = 2.5$ μm , and a source-gate spacing $L_{SG} = 500$ nm. The V-gate structure has a 110 nm-long top, 70° sloping side walls, a 40 nm-long footprint and a small metal lip formed on top of the 60 nm-thick Si_3N_4 that acts as a short field plate. DC measurements were performed using an HP 4142 (Fig. 1). The full-channel current at +1 V_{GS} was measured at 580 mA/mm, and the maximum transconductance $g_{m,\text{max}} = 220$ mS/mm at $V_{GS} = -1.8$ V. The measured pinch-off

voltage was -3.0 V. A slight, thermally-induced differential resistance was observed, which is attributed to the poor thermal conductivity of the air gap between the 75 μm free-standing diamond to the chuck [3]. Using an HP 8510XF, small signal measurements were performed through 100 GHz; a small inductance was observed above ~ 65 GHz. Fitting in the linear region of the results indicates a $f_T = 85$ GHz and $f_{\text{max}} = 95$ GHz (Fig. 2) in spite of a high 800 Ω/\square sheet resistance. These are the highest f_T and f_{max} values demonstrated for devices on GaN/D.

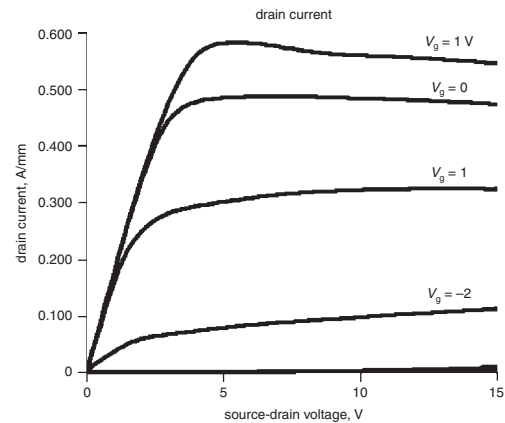


Fig. 1 I - V characteristic for $2 \times 50 \times 0.04$ μm GaN/D HEMT

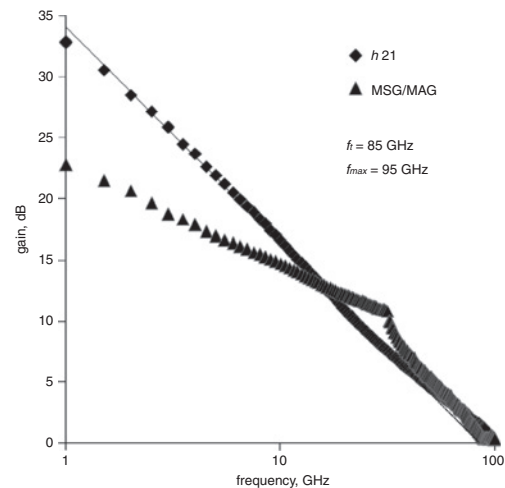


Fig. 2 h_{21} and MSG/MAG response for $2 \times 50 \times 0.04$ μm GaN/D HEMT, with best fit intercepts indicating $f_T = 85$ GHz and $f_{\text{max}} = 95$ GHz

Conclusion: A high-performance AlGaIn/GaN HEMT on diamond substrate is reported. Copper was utilised in the gate metal stack in an effort to reduce gate resistance and increase the frequency performance. The 40 nm device exhibited $f_T = 85$ GHz and $f_{\text{max}} = 95$ GHz.

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Q. Diduck, J. Felbinger and L.F. Eastman (Department of Electrical and Computer Engineering, Cornell University, 425 Phillips Hall, Ithaca, NY 14852, USA)

E-mail: diduck@ieee.org

D. Francis, J. Wasserbauer, F. Faili, D.I. Babić and F. Ejeckam (Group4 Labs, Inc., 1600 Adams Drive, Suite 112, Menlo Park, CA 94025, USA)

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