Development of Amplifier Modules based on GaN-on-diamond HEMTs

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Abstract—**X-band amplifier modules based on GaN-on-diamond high-electron mobility transistors have been demonstrated for the first time. In this paper we describe the GaN-on-diamond device design and fabrication, die processing, and the design and packaging of hybrid RF amplifier modules. Furthermore, thermal resistance measurements were performed on the amplifiers using liquid-crystal thermography and were shown to agree with theoretical predictions and previously published measurements on GaN-on-diamond devices.**

Index Terms—**Microwave power amplifiers, semiconductor device manufacture, MODFETs, microstrip circuits.**

I. Introduction

HEAT generated in electronic devices is the source of premature device failure and performance degradation. For these reasons, highly-efficient solid-state devices and optimal thermal management are critical elements to building reliable high-performance electronics, especially RF and mm-wave high-power amplifiers. Over the past decade, gallium-nitride (GaN) has entered commercial markets as the material of choice for high-power and high-frequency amplification due to its superior electronic properties. However, the performance of high-power components based on GaN is limited by the low thermal conductivity of the active materials (AlGaN/GaN) and the substrates on which the devices are grown. We have invented and developed a process that profoundly expands GaN chip thermal properties [1,2]: the process atomically attaches GaN epilayers to chemical-vapor-deposited (CVD) diamond wafers. The result is an engineered wafer with GaN-based active layers disposed on a CVD diamond substrate. Using this technology, we have successfully demonstrated high-electron mobility transistors (HEMT) with f_T ~ 85 GHz and 4 W/mm output power [3,4] and that the thermal resistance of GaN-on-diamond transistors is half that of similar GaN transistors grown on silicon carbide substrates [5]. Furthermore, the demonstration of full HEMT-wafer processing in this work and in reference [6] attest to the progress towards commercial viability of GaN-on-diamond technology and its use in light-weight, highly efficient, and reliable RF and mm-wave power amplifiers (PAs) for commercial, defense, and space applications. In this report, we describe the development of the first RF power amplifier modules based on GaN-on-diamond HEMTs operating in the X-band; we describe the complete process sequence starting with the engineered GaN-on-diamond wafers and ending with a connectorized amplifier module. The purpose of this work is to be an instructive guide for the HEMT and PA designer about GaN-on-diamond technology.

Developing electronic circuitry, and especially high-frequency solid-state amplifiers, in GaN-on-diamond technology is challenging because: (a) diamond substrates are very hard and difficult to micro-machine; wafers cannot be diced using traditional methods applied to silicon (Si), silicon carbide (SiC), and other compound semiconductors, (b) wafer thinning, although possible, is impractical primarily because diamond substrate cost is proportional to its thickness, (c) the fact that CVD diamond wafer cost scales with its thickness means that the GaN-on-diamond wafer thickness (selected prior to device fabrication) becomes the thickness of the final "production" chip. For monolithically integrated microwave integrated circuits (MMICs) chip thicknesses range between 50 and 100 μm. Most commercial foundries are not equipped to handle large wafers (e.g. 100 mm) thinner than several hundred micrometers because such free-standing wafers are fragile and can exhibit unacceptably high bow. To address this difficulty, we have developed a Si-wafer carrier to enable robust handling and processing of GaN-on-diamond wafers (50 mm, 75 mm, and 100 mm) in existing commercial foundries alongside other semiconductor wafers [7]. In this work, we used free-standing GaN-on-diamond substrates with size 15 x 15 mm².

II. Wafer, Device Design, Fabrication and Characterization

The epilayer structure used to make HEMTs was grown by metal-organic chemical-vapor deposition (MOCVD) on (111) Si substrates [8]. A proprietary nucleating layer was followed by an 800-nm unintentionally doped (UID) GaN buffer layer and a 17.5 nm $Al_{0.26}Ga_{0.74}N$ barrier layer which was capped with 2 nm UID GaN. This epilayer stack was first attached (face to face) to a sacrificial substrate so that its growth (111)

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Si substrate can be removed. Next, the exposed back of the GaN stack was atomically attached to a 100-µm thick chemical-vapor deposited (CVD) diamond substrate. This double transfer is necessary to preserve the GaN crystal orientation: Ga-face remains on top. Further details of the manufacturing of GaN-on-diamond wafers are given in references [1,2]. The 2DEG charge density was estimated from Mercury-probe C-V data to be $n_e \approx 7.3 \cdot 10^{12}/\text{cm}^2$, which with sheet resistivity $R_{SH} \approx 434$ Ω/sq (measured using TLM) yields low-field mobility $\mu_e = (e n_e R_{SH})^{-1} \approx 1{,}950$ cm²/Vs.

The smooth surface of the diamond wafer (the mandrel face) is adjacent to the GaN/AlGaN epilayers, while the rough surface of the diamond (growth face) forms the wafer back. The diamond substrates were grown using microwave plasma and exhibit columnar-grain growth with grain size of ≈ 20 µm at the growth surface. We measured the bulk heat conductivity (average value for the entire wafer) of diamond wafers used in this work to be $\kappa_D \approx 1{,}500$ W/cmK. The thermal conductivity of CVD grown diamond increases with the diamond thickness [9]. The diamond thickness is selected based on the expected dimension of the heat source: Optimal heat spreading occurs when the characteristic length/width of the heat source is comparable to the thickness of the heat spreader [2]. The HEMT gate width is chosen to be 100 µm and hence a 100-µm diamond thickness was used.

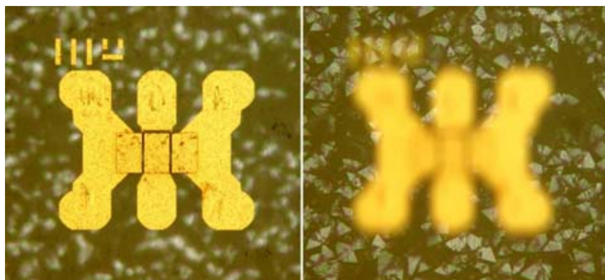

Fig. 1 – Image of 2 x 75 µm HEMT with focus on the device and focus on the back of the diamond wafer showing diamond crystals on the back surface (diamond is transparent)

The device fabrication consisted of six lithography steps, all currently done with E-beam lithography, but most can easily be implemented with optical lithography. The processed devices had two gate-fingers and no air-bridges. For devices with four or more gate-fingers, air-bridges are needed and this would add two additional lithography steps. Starting with the GaN-on-diamond wafers, the process begins with the creation of Ti-Pt alignment marks that are used for the alignment of subsequent layers and laser scribing. This is followed by ohmic metal deposition, 64-nm PECVD silicon nitride passivation deposited at 300°C, access to ohmic contact metal using CF4 reactive ion etch, mesa isolation using B/Cl_3 reactive ion etching, contact pads, and Ni/Au gates. Ohmic-contacts metal stack consisted Ta/Ti/Al/Mo/Au (12/15/90/45/50 nm). Ta/Ti combination is used to improve adhesion to GaN and to provide a large nitrogen solubility which facilitates the creation of nitrogen vacancies during the anneal process and hence a strong N+ region in the contact interface. Al establishes the contact when it dissolves in Ta/Ti and diffuses through the initial layers, while Mo acts as a barrier layer for the Au layer. The contact anneal is performed in a nitrogen atmosphere in a two step process: 700°C/60secs and then 800°C/20secs. The contacts and the epilayers were characterized by TLM. Sheet resistance of 434 Ω/sq ($3.8 \cdot 10^{-6}$ Ωcm^2), transfer length of 0.94 µm, and a contact resistance of 0.4 Ωmm were measured. The process for bonding pads involves a separate gate metallization which uses Ti-Au metallization. No substrate-thru vias were implemented at this time. As diamond substrates are insulating, there was no need for backside contact metallization, hence no metallization has been applied to the back of the wafers in this work. However, diamond back-surface does not wet in common solders and for solder mounting one will require a wetting-metallization layer, such as, Ti/Au deposited by sputtering. In the future, for RF and millimeter-wave MMICs, the traces on top of the chip will use either micro-strip or conductor-backed coplanar waveguide (CB-CPW) transmission lines. All such implementations will require back-of-wafer metallization and thru-via technology.

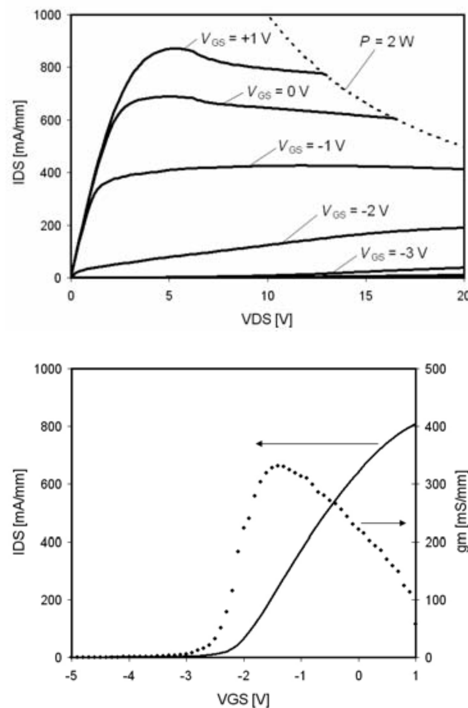

Fig. 2 – On-wafer DC measurements on run 129B

Devices with a variety of gate lengths (100 nm, 150 nm) and gate widths (150, 200, and 300 µm) were built. Other relevant HEMT dimensions were L_{GS} = 500 nm, L_{DG} = 2 µm, gate pitch 50 µm, and an overhang (field plate) on the Γ-shaped-gate of 60 nm. A finished 2 x 75-µm device is shown in Figure 1, with two focal depths showing the top surface of the wafer (focus on the device) and the bottom surface (focus

on the diamond back surface as seen though the wafer); both AlGaN/GaN epilayers and the diamond substrate are transparent to visible light. The transistors were laid out on a 600 x 600 µm grid to avoid any e-beam stitching errors (300 µm) in a rectangular 16 x 16 array (sample wafer size 15 x 15 mm²). Several wafers were processed, we focus on one (129B) to illustrate the development. RF coplanar probes were used to measure small-signal *s*-parameters, source/load pull, and DC performance on the wafer.

We chose a W_G = 2 x 100-µm device with L_G = 100 nm gate for amplifier design. This decision was based on the desire to optimize gain at 10 GHz (gate width around 100 µm is typically used for negligible phase error) and shortest gate length (higher transition frequency). Figure 2 shows example DC measurements. The negative slope in the saturation characteristics of the HEMT (Figure 2(a)) is due to heating. The thermal resistance of these transistors is around 33°C/W (see Section V for details). Therefore, at the 2-W boundary shown in Figure 2(a), the temperature rise between the device active area and the back of the wafer is more than 60°C above room temperature causing the pronounced drop in drain current at higher V_{DS} values.

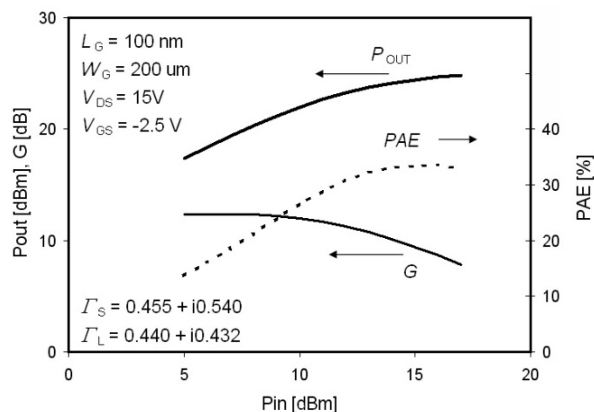

Fig. 3 – On-wafer power-in/power-out measurements on run 129B at 10 GHz.

The wafers were yielded by accepting devices that satisfy DC passing criteria: (a) for pinch-off: the devices can be shut off with resulting drain current less than I_{DS} < 2 mA/mm, and (b) for gate leakage: I_G < 1 mA/mm. Average maximum drain current of 830 mA/mm with standard deviation of 67, and transition frequency of 70 GHz was measured on 47 devices. Maximum drain current of 850 mA/mm is typical for GaN/Si HEMTs. The device breakdown voltage was greater than 30 V. Typical on-wafer-measured source/load-pull measurements are shown in Figure 3. The figure also lists the source and load impedances that were set to make the measurement. Best performance was exhibited at 15V bias for most devices. Analysis of input and output impedance on all devices at 10 GHz showed that that the small-signal input impedance can be modeled as a parallel $R_{GS}C_{GS}$ circuit with $R_{GS} \approx 3$ Ωmm and $C_{GS} \approx 0.6$ pF/mm of gate width, while the output parallel $R_{DS}C_{DS}$ circuit exhibits $R_{DS} \approx 36$ Ωmm and $C_{DS} \approx 0.3$ pF/mm of gate width.

III. Die Processing

The processed GaN-on-diamond wafers were laser-scribed and manually cleaved into 600 x 600 µm² chips. In the semiconductor industry, dicing is accomplished either by sawing of the wafer or scribing and cleaving the wafer into individual die. For single-crystal wafers (silicon and GaAs, for example), scribing and cleaving traditionally means separating wafers into die along crystallographic planes that naturally have weaker bonds. CVD diamond is polycrystalline and there is no one crystallographic plane along which the crystal may break to leave a flat edge; therefore, the weakening of the wafer has to be accomplished using laser micromachining. We *scribed* the GaN-on-diamond wafers by laser etching trenches in a rectangular (Manhattan) pattern. The laser-scribing was performed while the wafer was attached to standard dicing tape stretched on a hoop. The best results were obtained with medium tack dicing tape ("blue tape") [10]: it stretched easily and elastically which proved to be beneficial for efficient cleaving of diamond die. The tape has also proven to be very resilient during laser scribing, sustaining minimal damage in situations where the scribe was too deep. Figure 4 shows the side of a cleaved diamond wafer with the profile of a 60-µm deep laser-scribed trench. The AlGaN/GaN epilayers constitute the top 2 µm of the wafer shown in Figure 4, but cannot be resolved in this optical microscope image.

The laser drilling of diamond is a combination of thermal graphite ablation, which re-deposits graphite debris around the cut, and chemical etching in which graphite burns producing CO and CO_2 [10,11]. The balance between these two processes is strongly determined by the average laser power and the availability of oxygen. It is of critical importance that the laser scribing be debris-free because cleaning the graphite debris from individual die is quite difficult. In order to maintain a clean cut (no graphite redeposit), we adjusted the scribing conditions to burn (chemically etch) diamond by laser-scribing in oxygen atmosphere and to keep the laser average power at a level that produced little or no debris around the cuts. Laser cutting of diamond in oxygen also increases the laser cutting rate [12,13]. Furthermore, to minimize the heat damage, which increases the scribe alley width, we maintained laser pulse duration well below the thermal time constant of the diamond mass at the drilling location (estimated to be around 0.2 µs for a 25 µm beam spot) [15]. The typical scribing conditions on a Q-switched Nd:YAG 1064 nm laser were $P_{AVG} \leq 200$ mW, repetition frequency 1.5 kHz, beam speed 6.25 mm/s, and pulse duration: 35 ns to 60 ns [16]. Using this process we were successful in realizing 50-µm wide scribe alleys, although at least 80 µm is preferable for < 25-µm beam diameters.

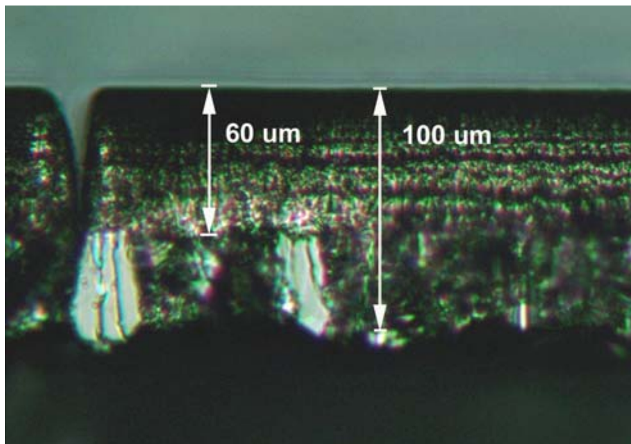

Fig. 4 – Side-view of a cleaved 100-µm GaN-on-diamond wafer. One un-cleaved scribe is visible; the scribe depth is 60 µm.

Wafer cleaving was done manually by pressing the dicing hoop with the blue tape against the rounded edges of a cleaving wedge. The ability to cleave a wafer using the cleaving wedge depends on the difference in torque that can be exerted on two adjacent die on the wafer. The smaller the die, the harder it is to cleave the wafer. Our experience is that the ratio between the smallest die dimension and the remaining uncut thickness of diamond should be at least 10:1 for an efficient cleave. It is important to note that the cut should not be allowed to come too close to the rough back side of the diamond because the uneven back surface will cause a significant weakening in the wafer and the wafer may break during scribing, impacting the alignment. For 100-µm diamond thickness used in this work, the remaining uncut thickness was kept above 30 µm. Breaking large un-scribed sections of the wafers produces diamond dust which can easily land on the surface of the die and scratch the device metallization. For this reason, the remaining thickness to be broken should be kept as small as possible. The two HEMT wafers used in this work were scribed to a 60 µm depth (diamond thickness is ~100 µm).

Finally, in order to be packaged and treated on the same footing as other present-day microwave and millimeter-wave integrated circuits, GaN-on-diamond chips will eventually provide a back-side contact for mounting and return path. This is planned to be accomplished with metal-coated thru vias that will connect the top source electrodes to the metalized back of the wafer using a process and recipe based on the above-described laser scribing.

IV. Amplifier Build

We designed a single-stage hybrid amplifier with one HEMT mounted on a copper-clad duroid® substrate. The tuning and bias networks were placed on a microwave substrate, while the substrate was inserted either into an RF test-fixture or packaged into an in-house developed high-thermal-conductance package (described in the next section). The microwave substrates consisted of a 125-µm thick RT/duroid® 5880 dielectric [17] with $\varepsilon_r = 2.2$ and $\tan(\delta) = 0.0009$ at 10 GHz attached to 1-mm thick copper plate, commonly referred to as "hard-clad duroid". Copper-clad duroid was chosen to achieve a simple mechanical design and assembly. We preferred a single substrate that can be inserted into a package while requiring only one mechanical tolerance: the distance from the input to the output RF plane. We furthermore wanted to mount the transistor chip directly on a metal heatsink (electrical ground) while keeping its top surface at a height approximately same as the electrical traces on top of the duroid to minimize bondwire length. Hard-clad duroid with dielectric thickness comparable to the die thickness was perfect for this type of arrangement: Milling out the dielectric in the center of the substrate and gold-plating it realized good electrical and thermal contact to the substrate, while the bondwire ends were almost level.

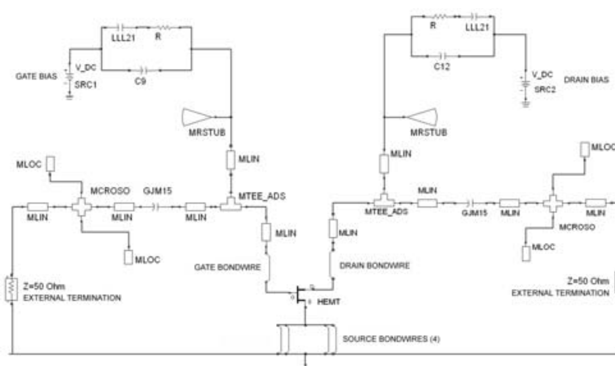

Fig. 5 – Amplifier circuit diagram (Agilent ADS)

The amplifier design was performed using ADS [18]. ADS device models were not available for these HEMTs, thus no Process Design Kit could be used. To work around this, the design was based on small-signal and load/source pull measurements obtained on a previous run with same transistor design. This run, referred to as run 057, featured $f_T \sim 57 \pm 2$ GHz, $I_{DSMAX} \sim 790$ mA/mm, breakdown voltage greater than 70 V, and about 20% dispersion [3]. The 057 devices were characterized at $V_{DS} = 35$ V and $I_{DS} = 10$ mA; the source and load terminations for maximum power were $\Gamma_S = 0.259 + i0.610$ and $\Gamma_L = 0.799 + i0.061$, respectively. The input match was realized as an L-match with an inductor formed by the gate terminal bond-wire plus the DC blocking capacitor parasitic inductance, and a shunt capacitor former by open ended stubs. The chip capacitor model was obtained from the manufacturer [19]. Wire-bonding was done using 1-mil gold wire. The real part of the output impedance was around 400 Ω. In order to create a λ/4 transformation from 50 Ω to 400 Ω needed to match the desired output matching impedance, one would need a 2-µm wide transmission line which is impractical. To avoid this, we first transformed 50 Ω to ~20 Ω using an open ended stub parallel to 50 Ω and the parasitic series inductor of the DC blocking cap. We then used an 89 Ω, quarter-wavelength transmission line (125 µm width) to transform this to 400 Ω. The drain-terminal bond wire model

was included in the output match. The amplifier circuit model is shown in Fig. 5.

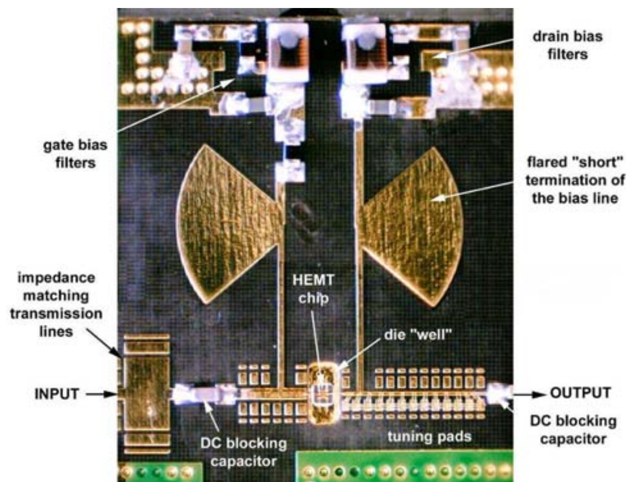

Fig. 6 – Top view of completed X-band amplifier

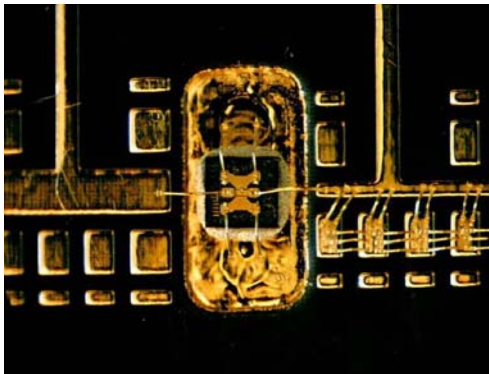

Fig. 7 – Close up image of the GaN-on-diamond HEMT with 200-μm gate periphery mounted in the amplifier shown in Fig. 6.

The bias circuit was designed to exhibit a parallel impedance of more than 1 kΩ over the frequency of interest and is included in the match. The stability was confirmed for the entire frequency range from 100 MHz to 15 GHz. The substrates also included tuning pads for fine adjustment. The expected peak power was 800 mW CW.

The HEMT chip was attached to the substrate using H20 epoxy [20]. The ground pads (source pads) were wire-bonded to the ground on the substrate with four bondwires. We applied wedge-bonding to all of our bonding in an attempt to minimize the bond-wire length (the inductance of the bondwires was modeled and included in the design). Figures 6 and 7 show magnified images of the completed hybrid amplifiers.

The mechanical format of our amplifier substrate (1.0” x 0.8”) allowed assembly for characterization by mounting coplanar end-launch connectors [21] to it (mechanical contact from the top; no soldering) and then attaching the substrate to an in-house designed 2” x 2” heatsink with fins that allow forced air cooling. This is practical for characterizing small quantities of amplifier substrates as the connectors need to be mounted for each test. Over 20 amplifiers were assembled and tested.

Fig. 8 – Completed amplifier modules

We designed a high-thermal-conductance microwave package, shown in Fig. 8, into which we placed the amplifier substrates. This package features a coplanar microwave transition between the traces on top of the substrate and the microwave end-connectors. The approach does not require strict machining tolerances and simultaneously offers (i) pressurized mechanical/electrical contact between the package/connectors and the substrate transmission lines, and (ii) heat path from the die to the bottom surface of the package via direct pressurized mechanical contact. Completed amplifier modules feature SMA connectors [21] and DC filter-terminals for gate and drain bias. The dimensions of the package are 1.39” x 1.29” x 0.39”; the material is aluminum with copper bottom heatsink.

The amplifiers were tested in Class AB operation. The performance was best between 8.7 and 8.9 GHz with small-signal gain exceeding 16 dB and return loss better than −6 dB. Figure 9 shows typical small-signal measurements. The highest output power obtained was 380 mW with PAE > 35% at 15V supply voltage (see Figure 10). This output power is equivalent to 1.9 W/mm. Maximum PAE of 42% was recorded for a different amplifier. The deviation from the design frequency and expected peak power is primarily due to difference in the performance of (a) the devices whose RF parameters were used to design the amplifier (057) and (b) the devices that were actually installed onto the amplifier substrates. The key difference was in the breakdown voltage, which was substantially lower on 129B relative to run 057. The cause of this reduction is attributed to process problems and are correctable through improved device process (e.g. different passivation) and design (e.g. epilayer structure, device geometry). Both device runs (057/129B) suffered from dispersion – about 20-30% difference between pulsed and DC output characteristics; this was confirmed by a separate measurement. Finally, we observed that the best amplifier modules performed better than best HEMTs measured on the wafer. We attribute this to better device heat sinking in the amplifier module.

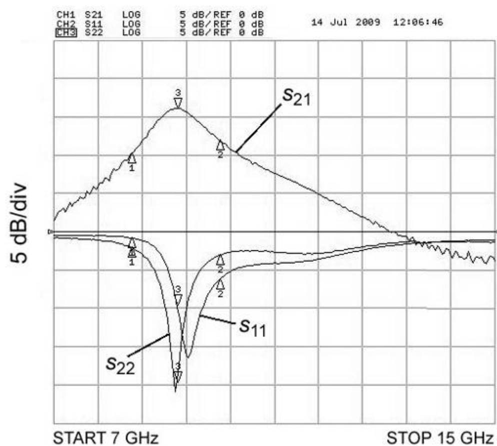

Fig. 9 – Typical small-signal measurements on run 129B

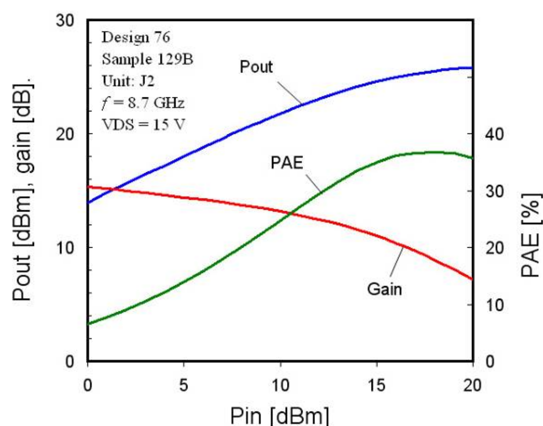

Fig. 10 – Amplifier biased for highest output power at 10 GHz

V. Thermal Resistance

The most desirable attribute of diamond substrates is their efficiency in spreading heat and lowering the device thermal resistance. To this end we measured the thermal resistance of fabricated amplifiers using liquid crystal thermography. An amplifier substrate was placed on a hot-plate and a thermocouple was attached to its corner to monitor its temperature. Only drain and source terminal of the HEMT were connected to a variable current source to deliver heating power. The dissipated power was measured using a voltmeter and an ammeter. A small quantity of nematic liquid crystal was then melted over the HEMT; the entire HEMT was immersed in the liquid crystal and the crystal phase-transitioned to liquid at the melting temperature (in this case 104°C). We used a nematic liquid crystal: 4-*n*-hexyloxybenzoic acid (CAS 1142-39-8) [22] and observed the nematic-isotropic (N-I) transition at T_{LC} = 153°C. Polarized light was incident on the HEMT and the liquid crystal and the reflection was observed using a microscope through another polarizer (analyzer). The analyzer was adjusted to be 90° away from the polarization of the light incident on the HEMT. For temperatures below the N-I transition of the liquid crystal the reflection is bright. Once the temperature of any part of the HEMT reaches the N-I transition temperature those regions become dark, and so mark the areas that reached the N-I transition temperature. To make the measurement, we varied the hotplate temperature and for each setting we found the amount of power required to bring the center of the chip to the N-I transition temperature. The electrical power is given by $P(T_{HS}) = (T_{LC}-T_{HS})/\Theta_{TH}$. From here, we set T_{HS}, then measured P and determined the thermal resistance Θ_{TH}. The measured thermal resistance was $\Theta_{TH} \approx 33$°C/W.

We also compared this result to the previously published measurements of thermal resistance of GaN/SiC and GaN-on-diamond HEMTs with similar dimensions using ThermoMicroscopes AFM-based SThM system[5]. In Ref. 5, GaN-on-diamond and GaN-on-SiC HEMTs exhibited $\Theta_{TH} \approx$ 30°C/W and $\Theta_{TH} \approx$ 60°C/W thermal resistance, respectively. The comparison between the data obtained in this work and reference [5] is shown in Figure 11. The excellent match between these measurements confirms that diamond substrates indeed have an advantage over silicon carbide substrates by factor of two in thermal conductance.

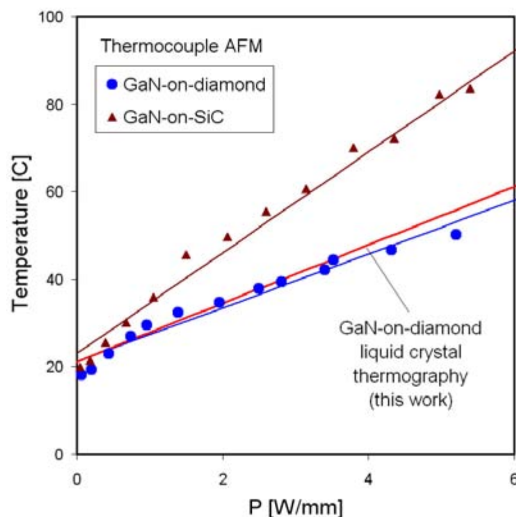

Fig. 11 – Comparison between the thermal-resistance measurements using Liquid Crystal Thermography in this work with the measurements reported in ref [5] where GaN/SiC and GaN-on-diamond were compared using AFM-based thermal resistance measurement.

We also compared this measurement to theory using a 3D finite-difference thermal solver. We used assumed 40-µm thick epoxy with κ_{epoxy} = 0.29 W/cmK [20] and calculate thermal resistance $\Theta_{TH} \approx 29$°C/W which is within 15% of the measured value. This theoretical analysis shows that the thermal resistance is dominated by the AlGaN/GaN layers and the epoxy rather than the diamond thermal conductivity, namely, most of the temperature drop occurs in the GaN/AlGaN layers (>50%) and the epoxy layer (~%20). The fraction of thermal resistance contributed by the epoxy will be reduced when the epoxy is replaced with AuSn solder.

VI. Conclusion

We have successfully demonstrated a complete amplifier module fabrication sequence with our GaN-on-diamond HEMT chips: from wafer and device fabrication, through wafer scribing and cleaving, pick-and-place, assembly, and packaging. Thermal resistance measurements on the same amplifier substrates confirm that diamond heat-spreading and lower thermal-conductance packaging will give a designer of GaN-based high-power microwave components thermal management solutions that are superior to any other available technology on the market.

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